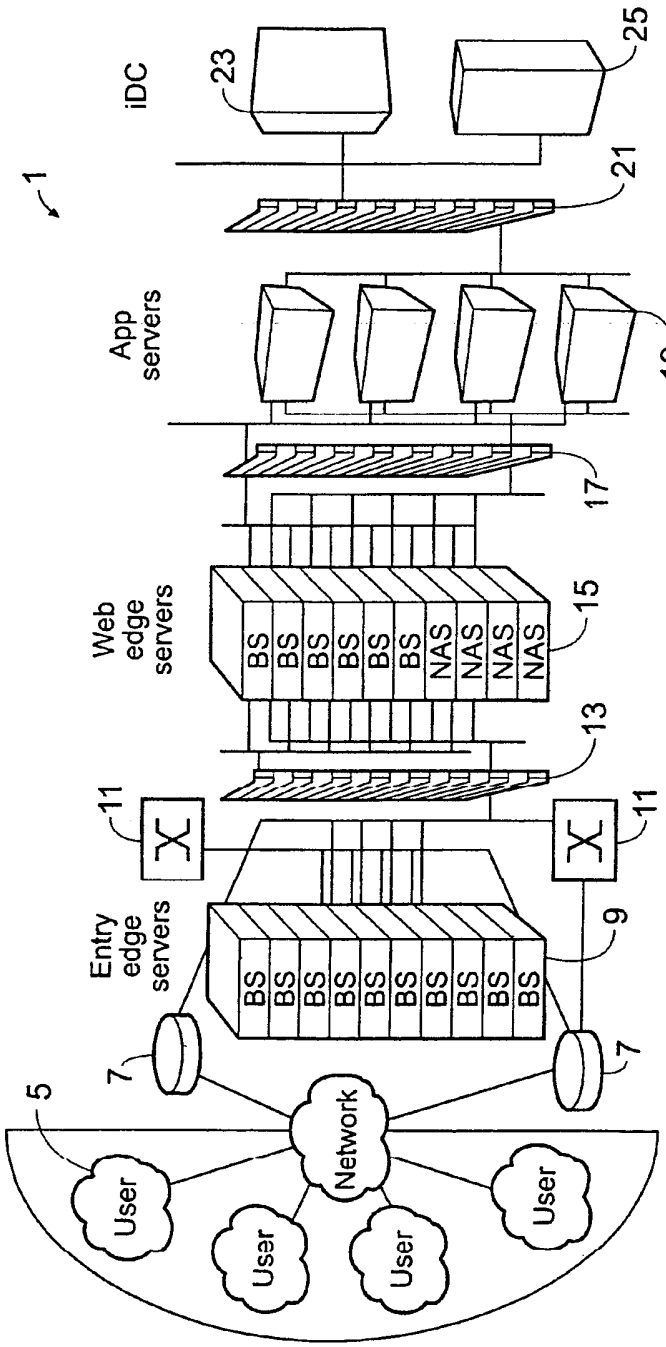

1
iDC
23
25
21
App servers
19
17
Web edge servers
BS
NAS
15
13
11
11
Entry edge servers
BS
9
7
7
5
Network
User
User
User
User

Fig. 1

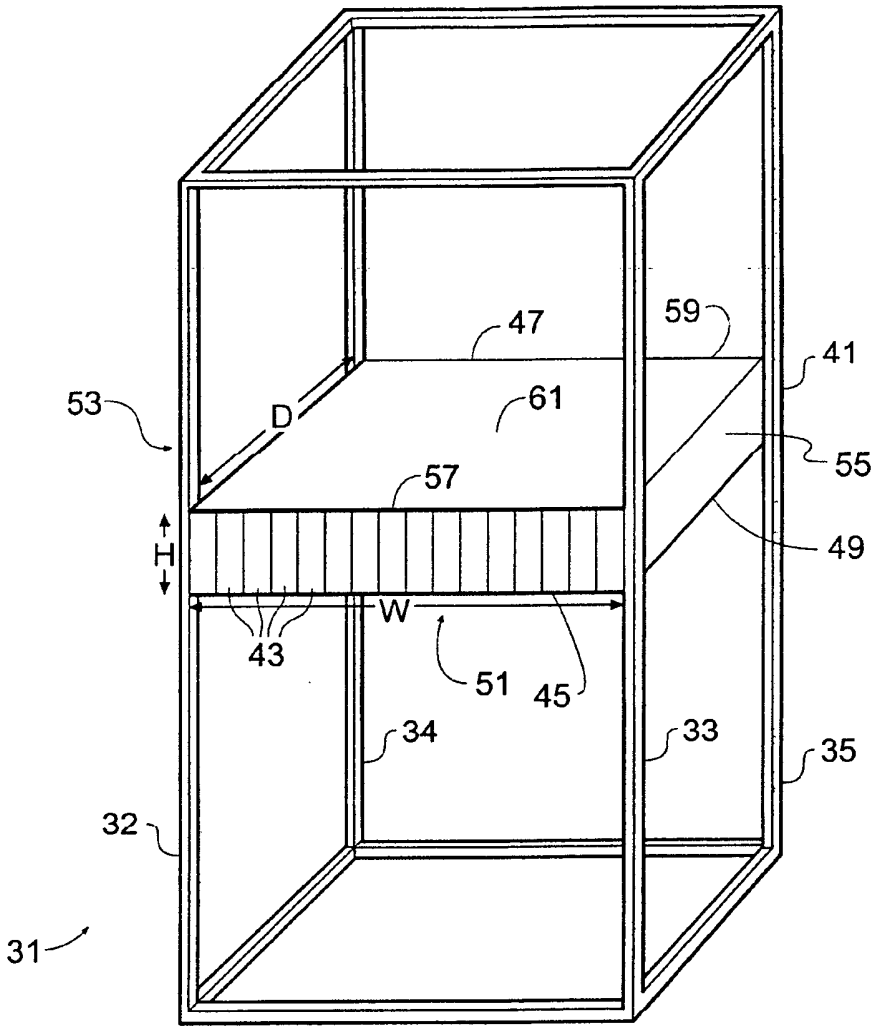


Fig. 2

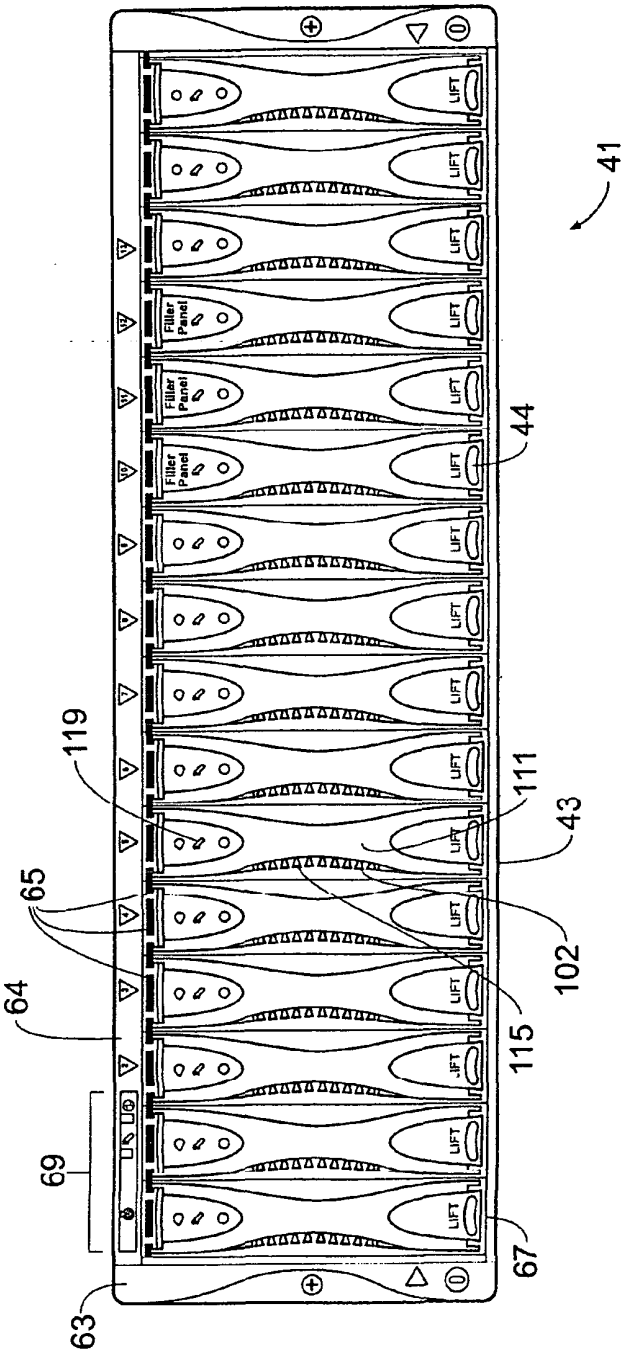


Fig. 3

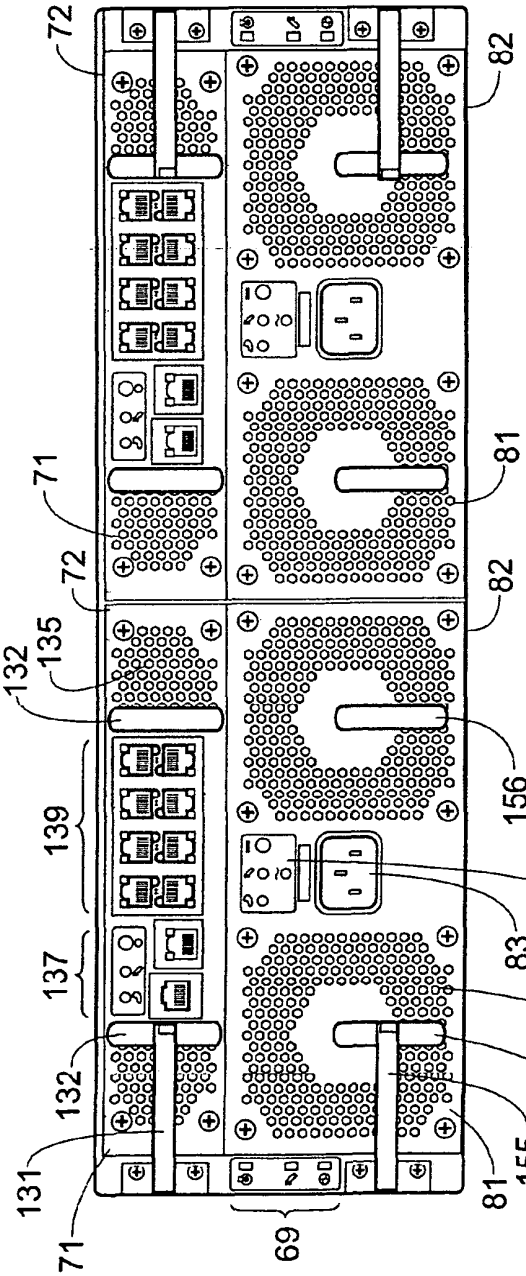

72
82
71
81
72
82
132
135
156
139
161
83
137
159
132
156
155
131
81
71
69

Fig. 4

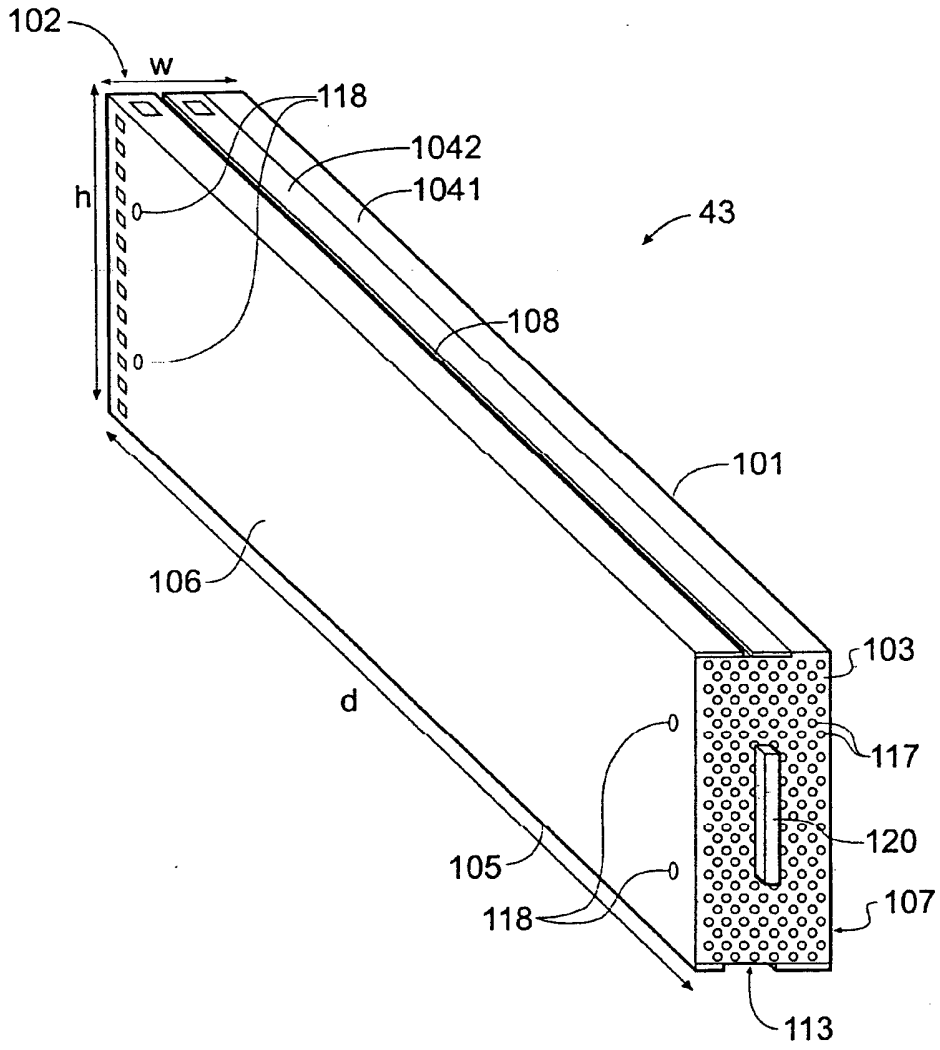


Fig. 5A

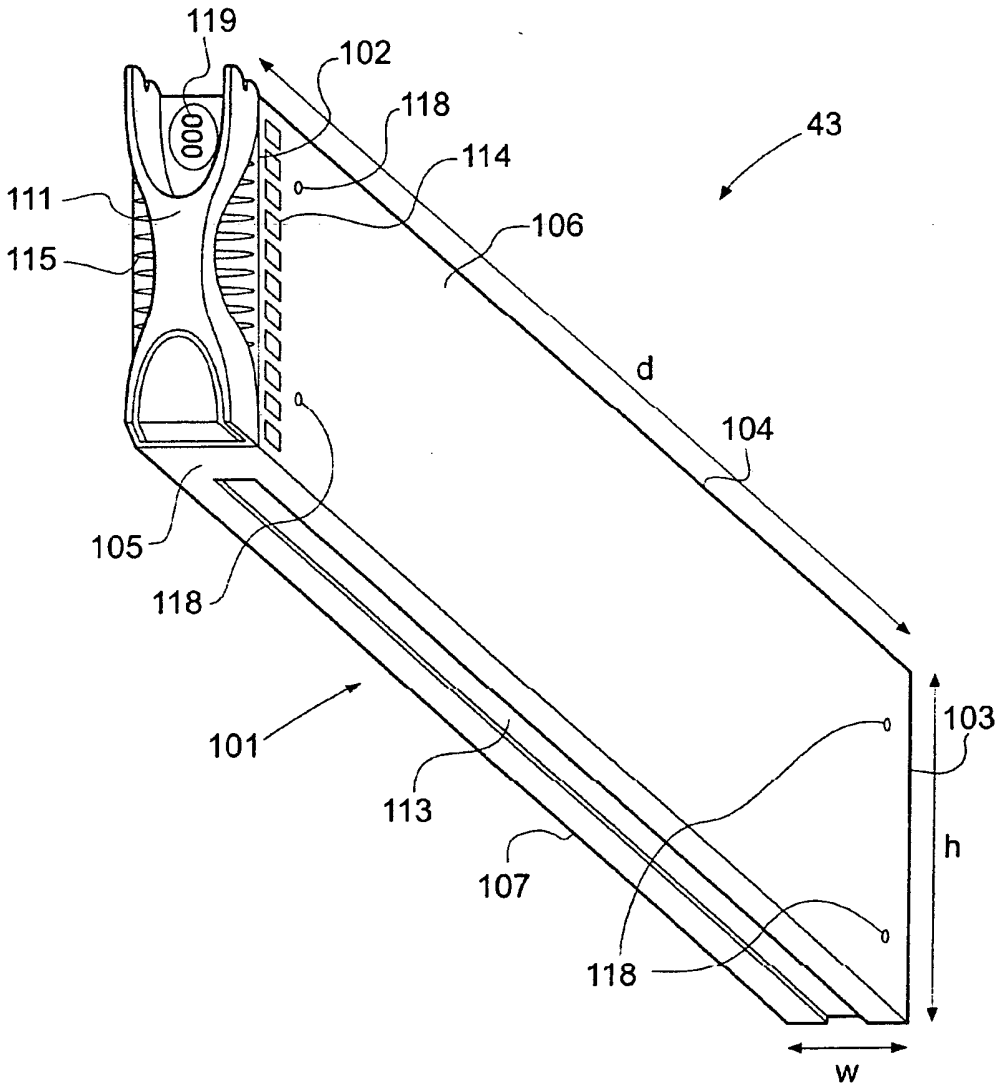

119
102
118
43
114
111
106
115
d
104
105
118
101
103
113
h
107
118
w

Fig. 5B

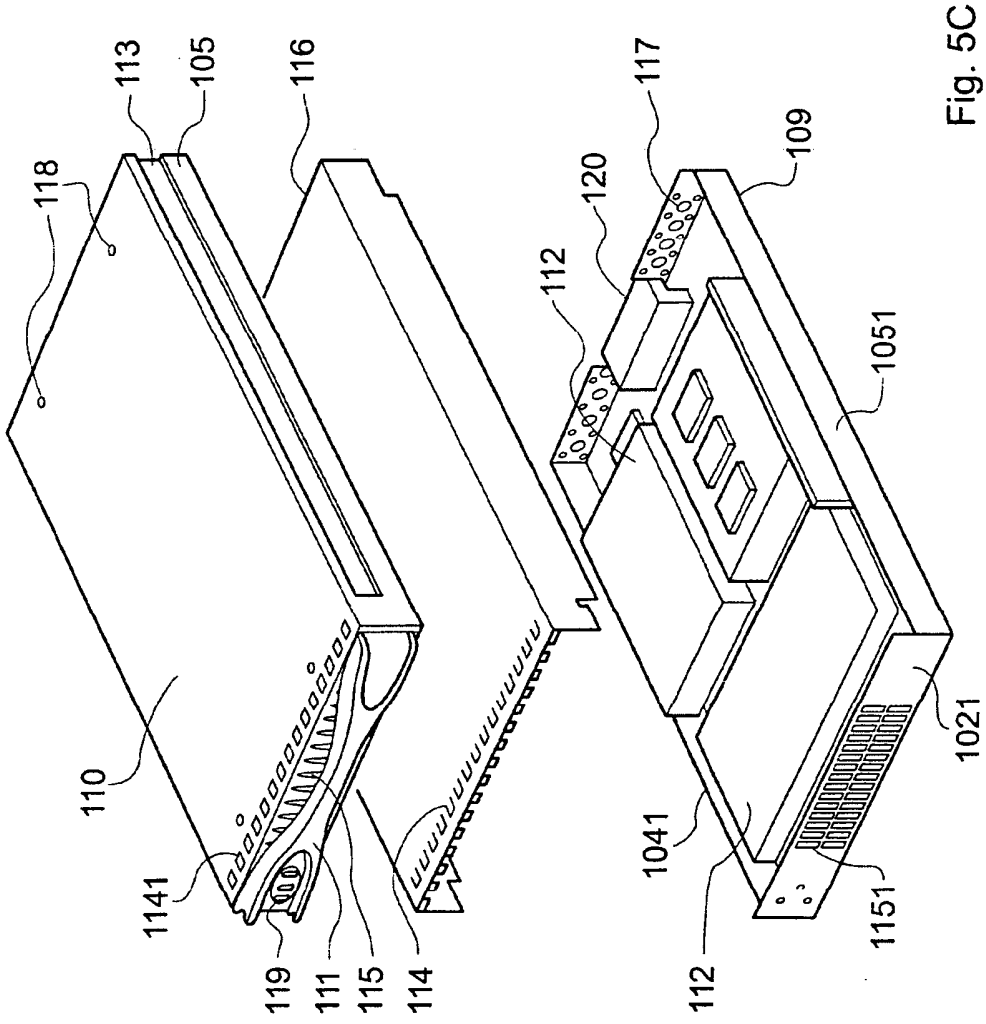

113
105
116
118
117
109
120
112
1051
110
1141
1041
1021
119
111
115
114
112
1151

Fig. 5C

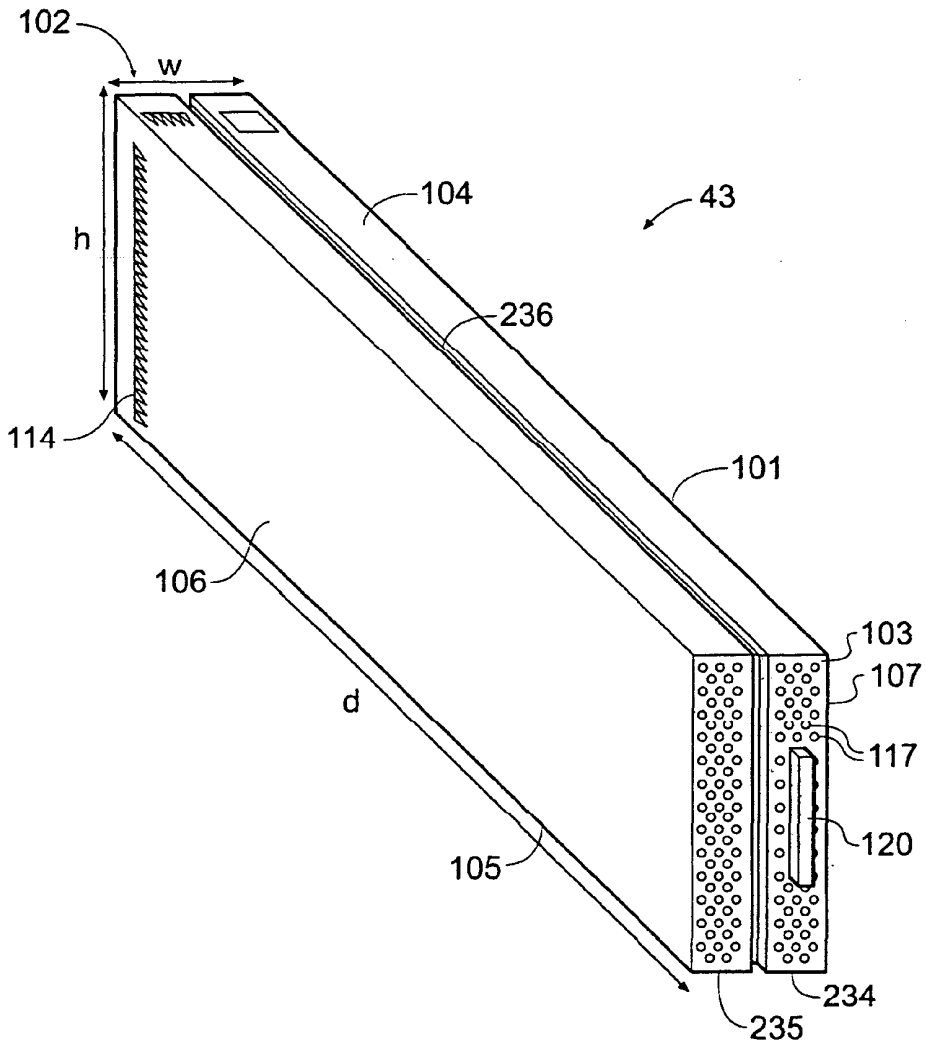


Fig. 5D

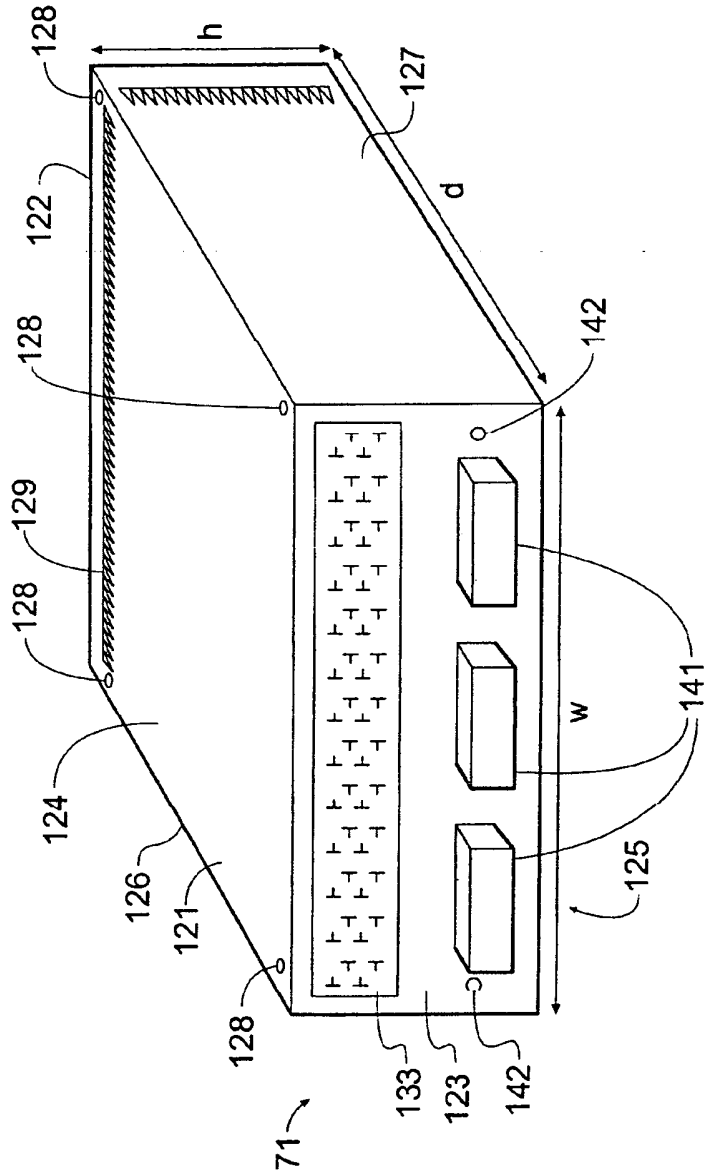

128
h
127
122
d
128
142
129
128
124
126
121
128
133
123
142
71
141
w
125

Fig. 6

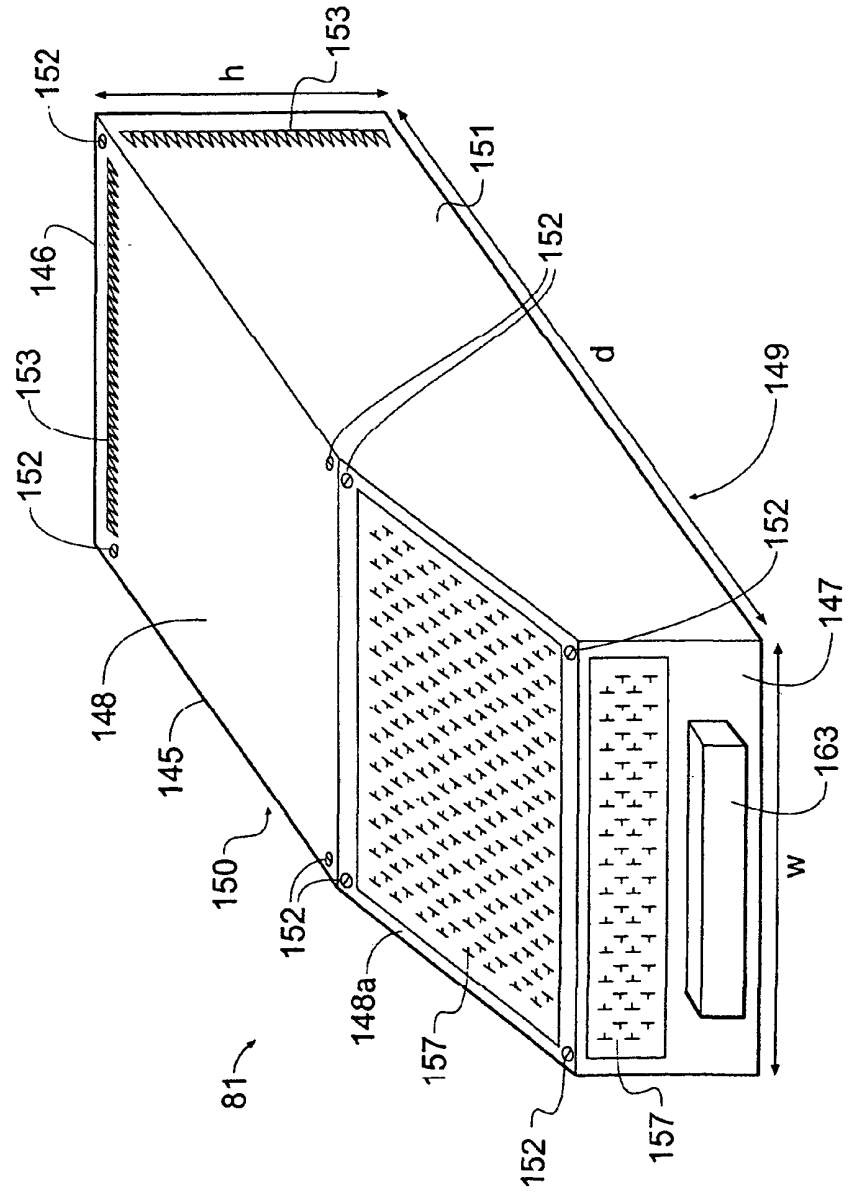

152
h
153
151
152
146
153
d
149
152
152
147
148
145
163
150
152
w
148a
157
81
152
157

Fig. 7

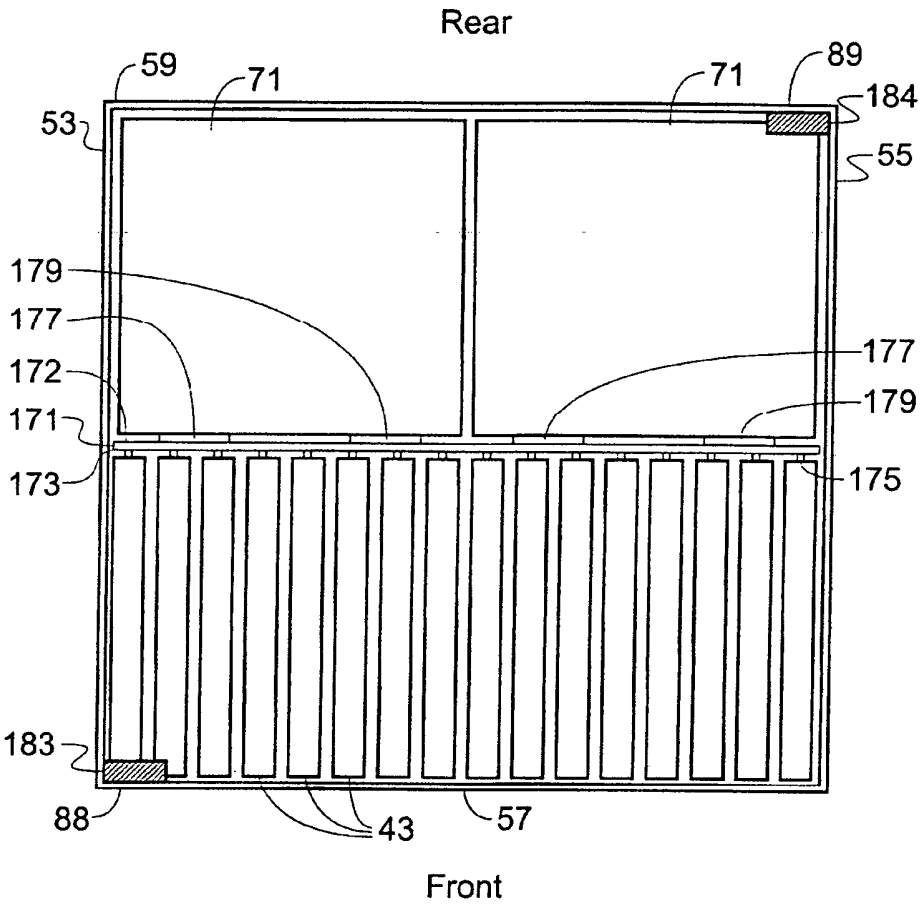

Rear
59
71
71
89
184
53
55
179
177
177
172
179
171
173
175
183
88
43
57
Front

Fig. 8A

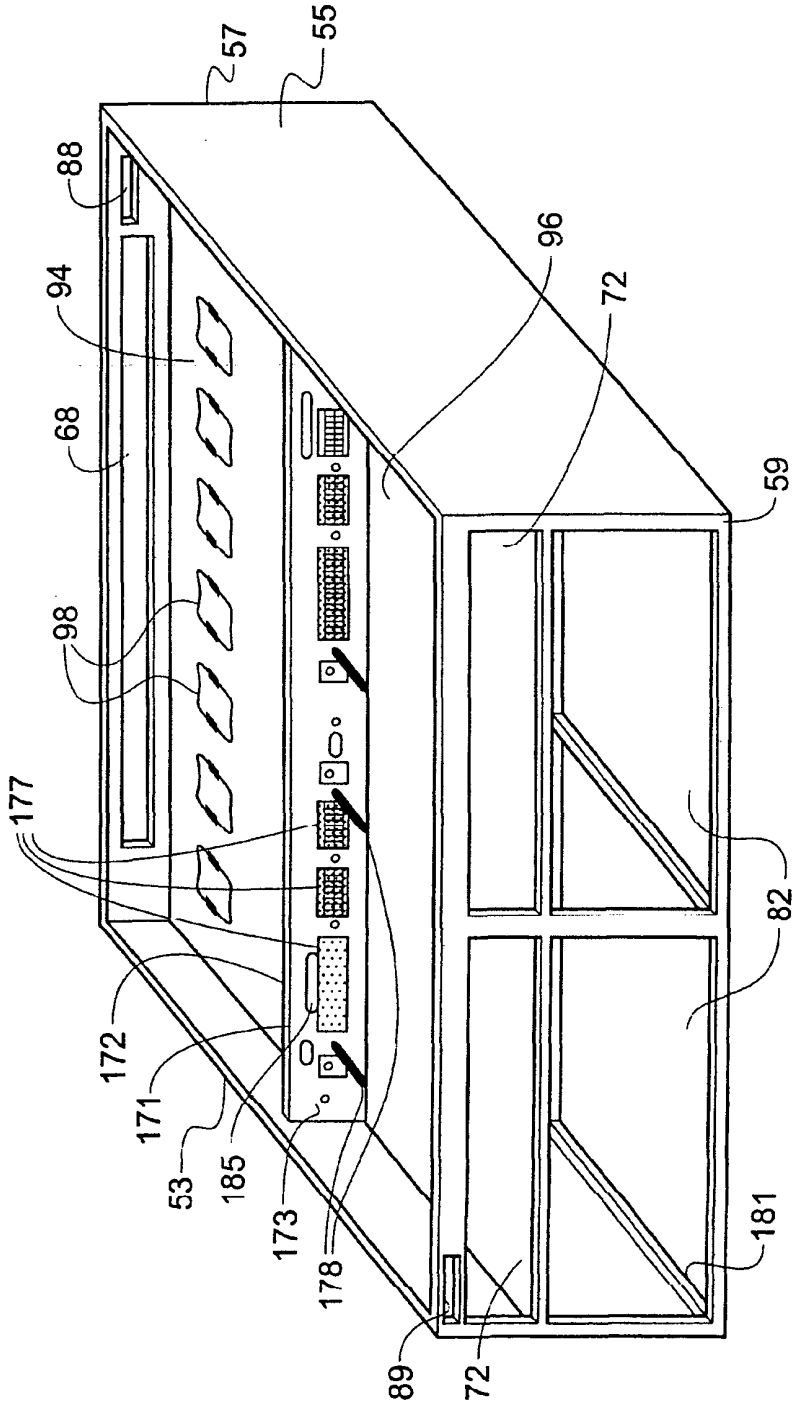


Fig. 8B

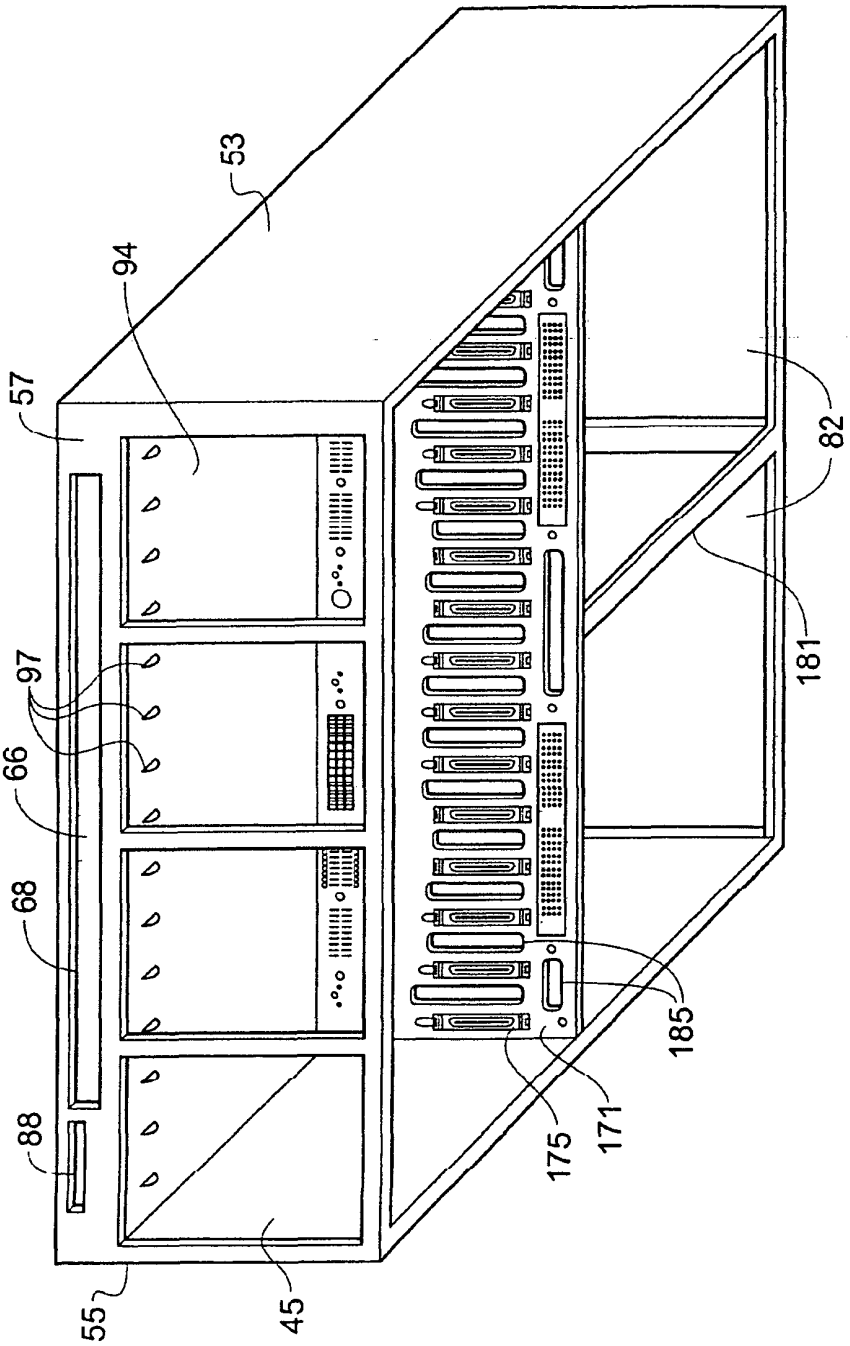


Fig. 8C

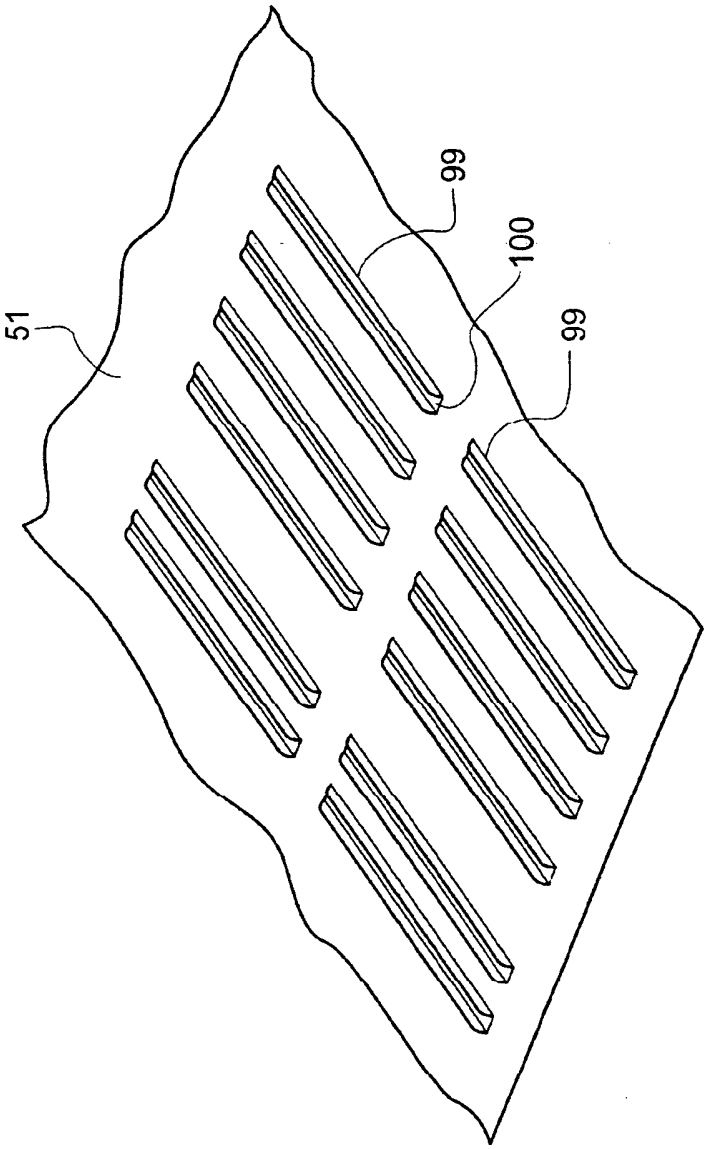


Fig. 8D

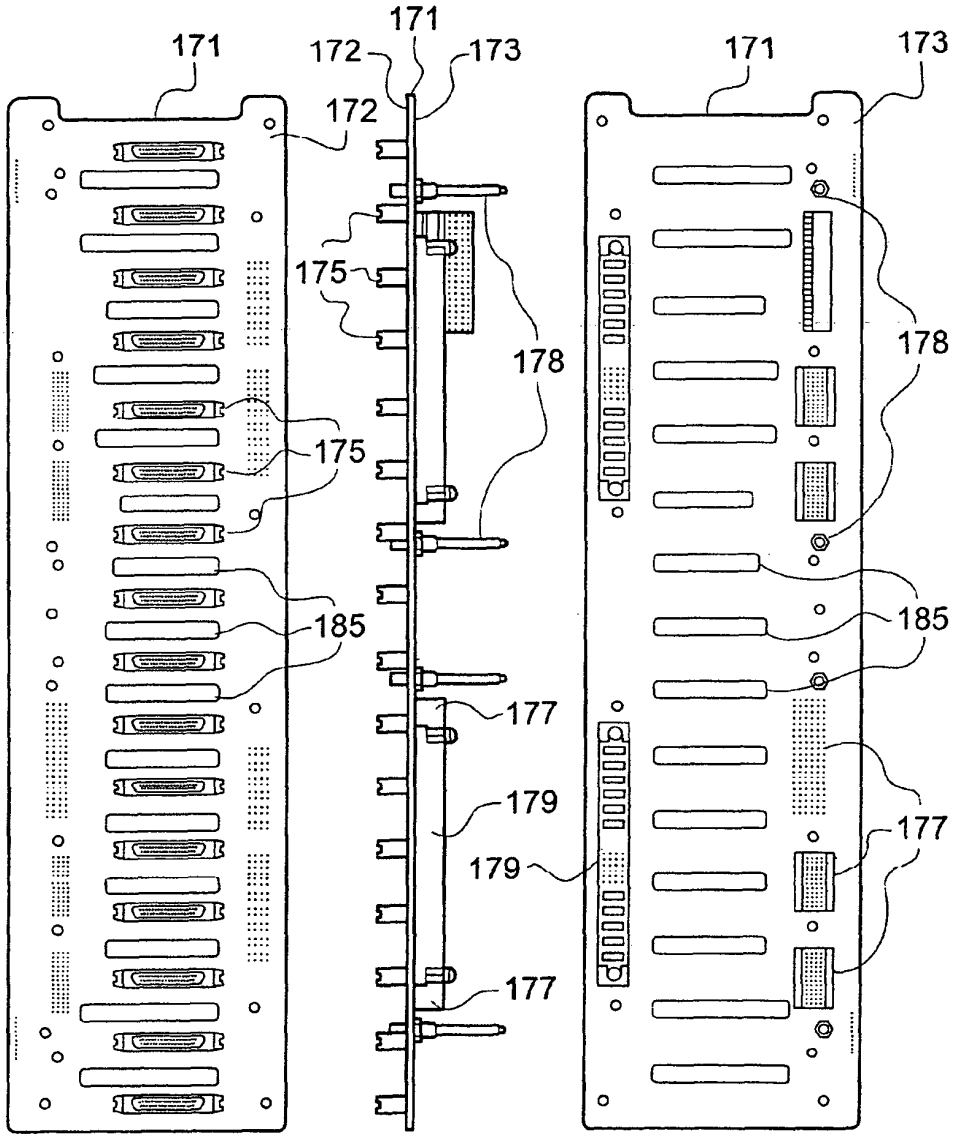


Fig. 9A Fig. 9B Fig. 9C

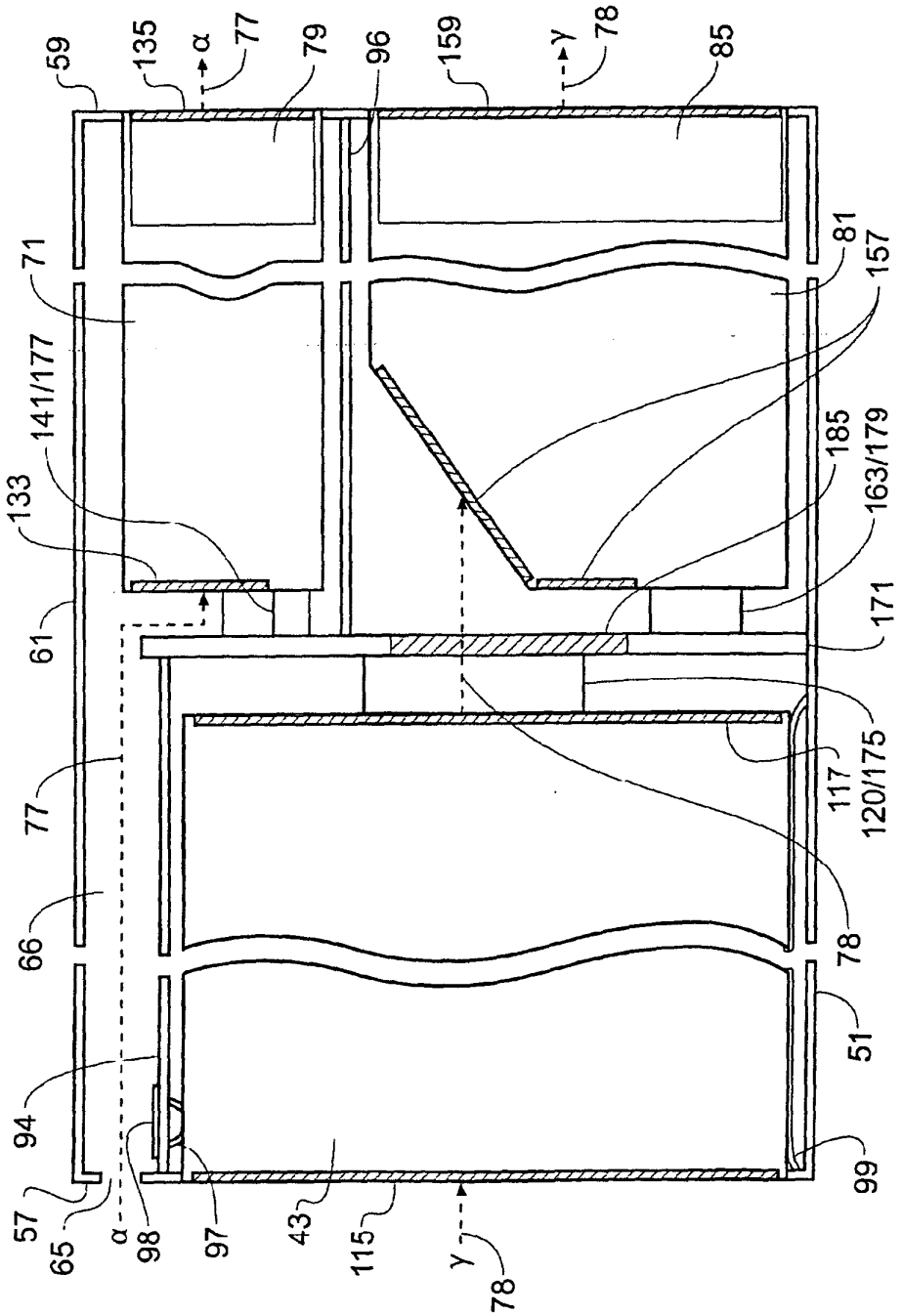

59
135
α
77
79
96
159
γ
78
85
71
81
157
141/177
185
133
163/179
61
171
77
117
120/175
66
78
94
51
57
65
α
98
97
43
115
γ
78
99

Fig. 10

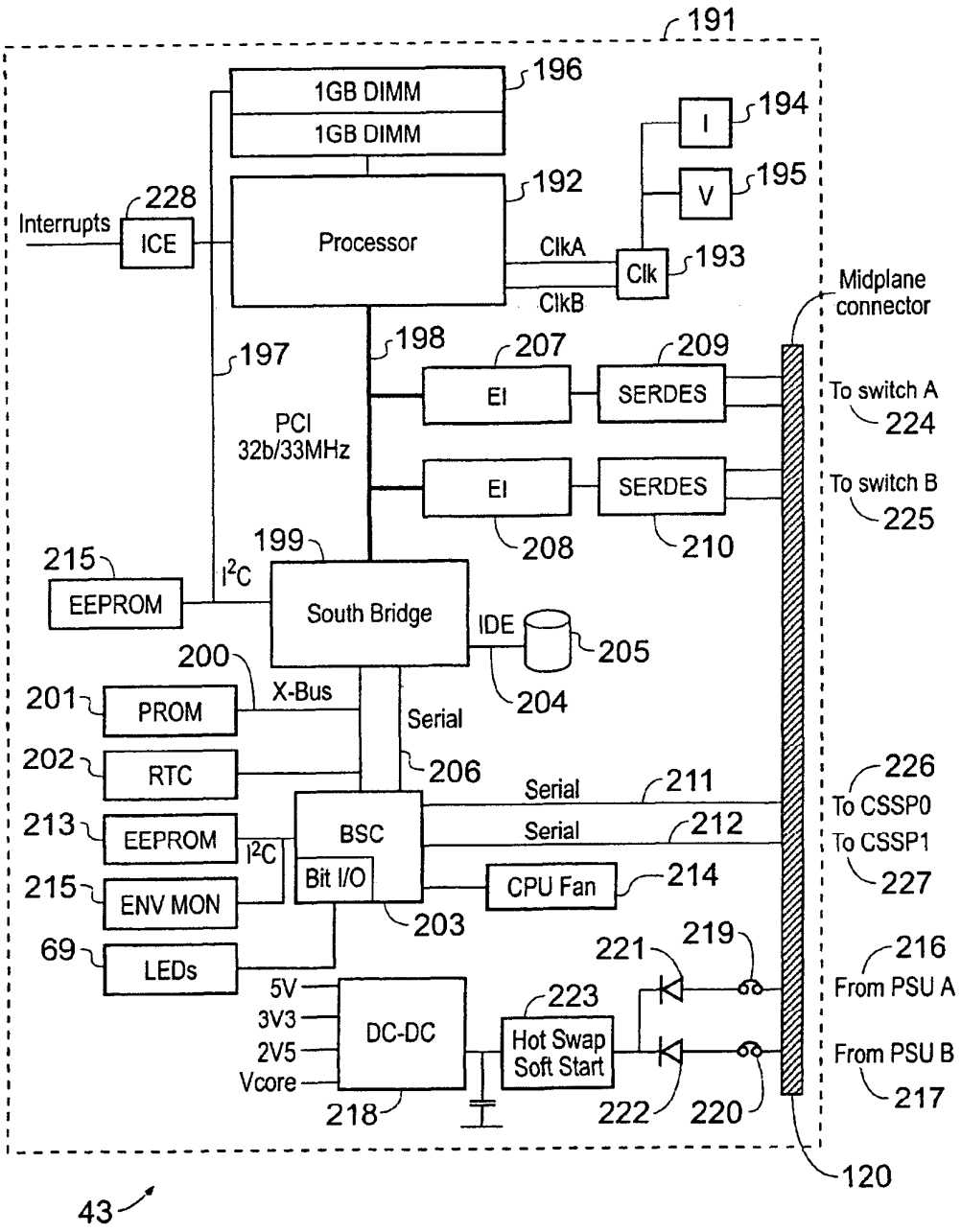
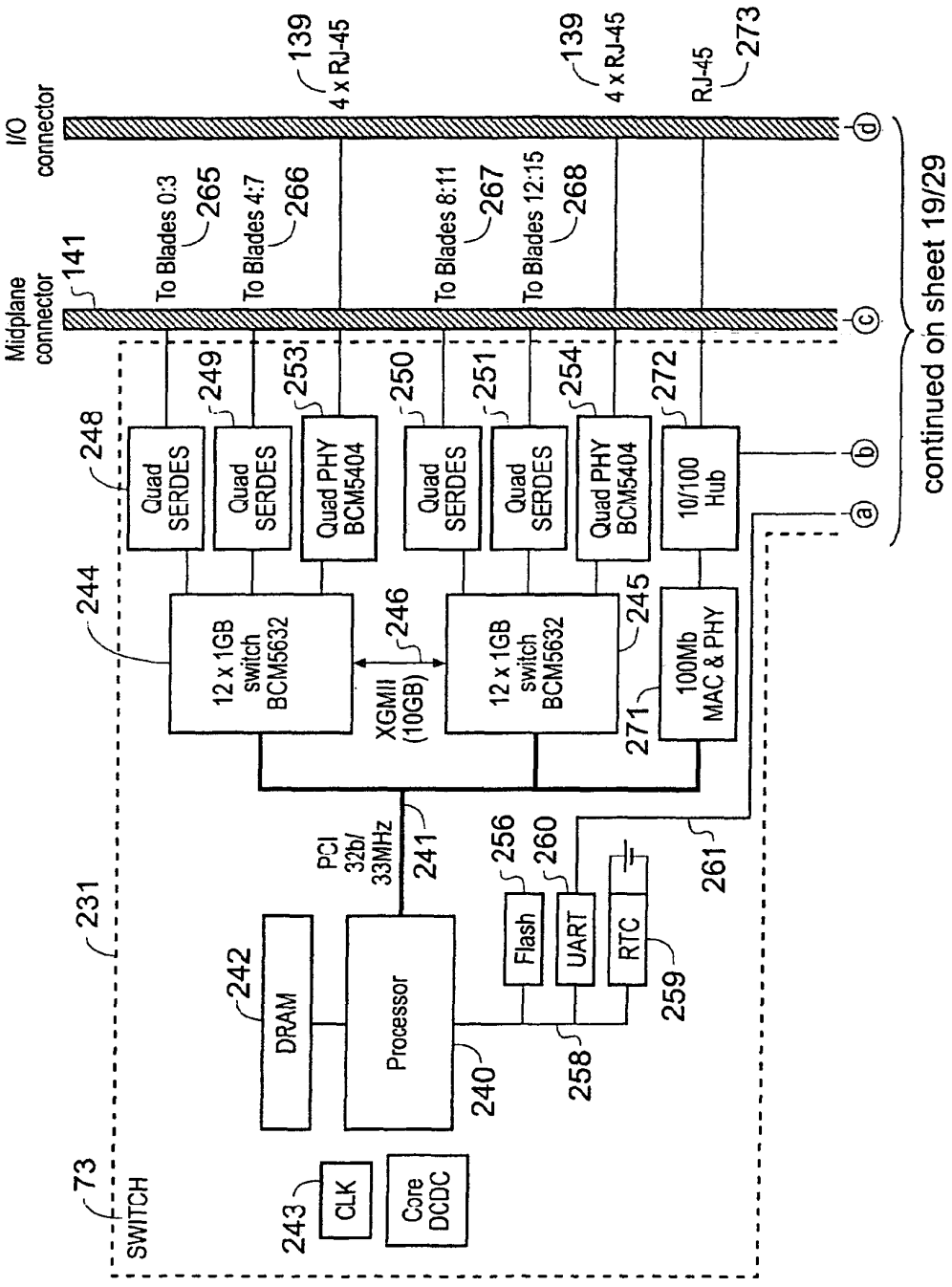

191
1GB DIMM
1GB DIMM
196
I
194
V
195
Processor
192
ClkA
ClkB
Clk
193
Interrupts
228
ICE
Midplane connector
197
198
207
209
EI
SERDES
PCI 32b/33MHz
To switch A
224
EI
SERDES
To switch B
225
208
210
215
EEPROM
I2C
199
South Bridge
IDE
205
204
200
X-Bus
Serial
201
PROM
202
RTC
206
Serial
211
226
To CSSP0
To CSSP1
227
213
EEPROM
I2C
BSC
Bit I/O
Serial
212
CPU Fan
214
215
ENV MON
203
69
LEDs
221
219
216
From PSU A
5V
3V3
2V5
Vcore
DC-DC
223
Hot Swap Soft Start
From PSU B
217
218
222
220
120
43

Fig. 11


I/O connector
Midplane connector
141
139
4 x RJ-45
139
4 x RJ-45
RJ-45
273
To Blades 0:3
265
To Blades 4:7
266
To Blades 8:11
267
To Blades 12:15
268
continued on sheet 19/29
248
249
253
250
251
254
272
Quad SERDES
Quad SERDES
Quad PHY BCM5404
Quad SERDES
Quad SERDES
Quad PHY BCM5404
10/100 Hub
244
12 x 1GB switch BCM5632
246
XGMII (10GB)
12 x 1GB switch BCM5632
245
100Mb MAC & PHY
271
PCI 32b/ 33MHz
241
261
231
256
260
242
DRAM
Processor
Flash
UART
RTC
259
240
258
73
SWITCH
243
CLK
Core DCDC

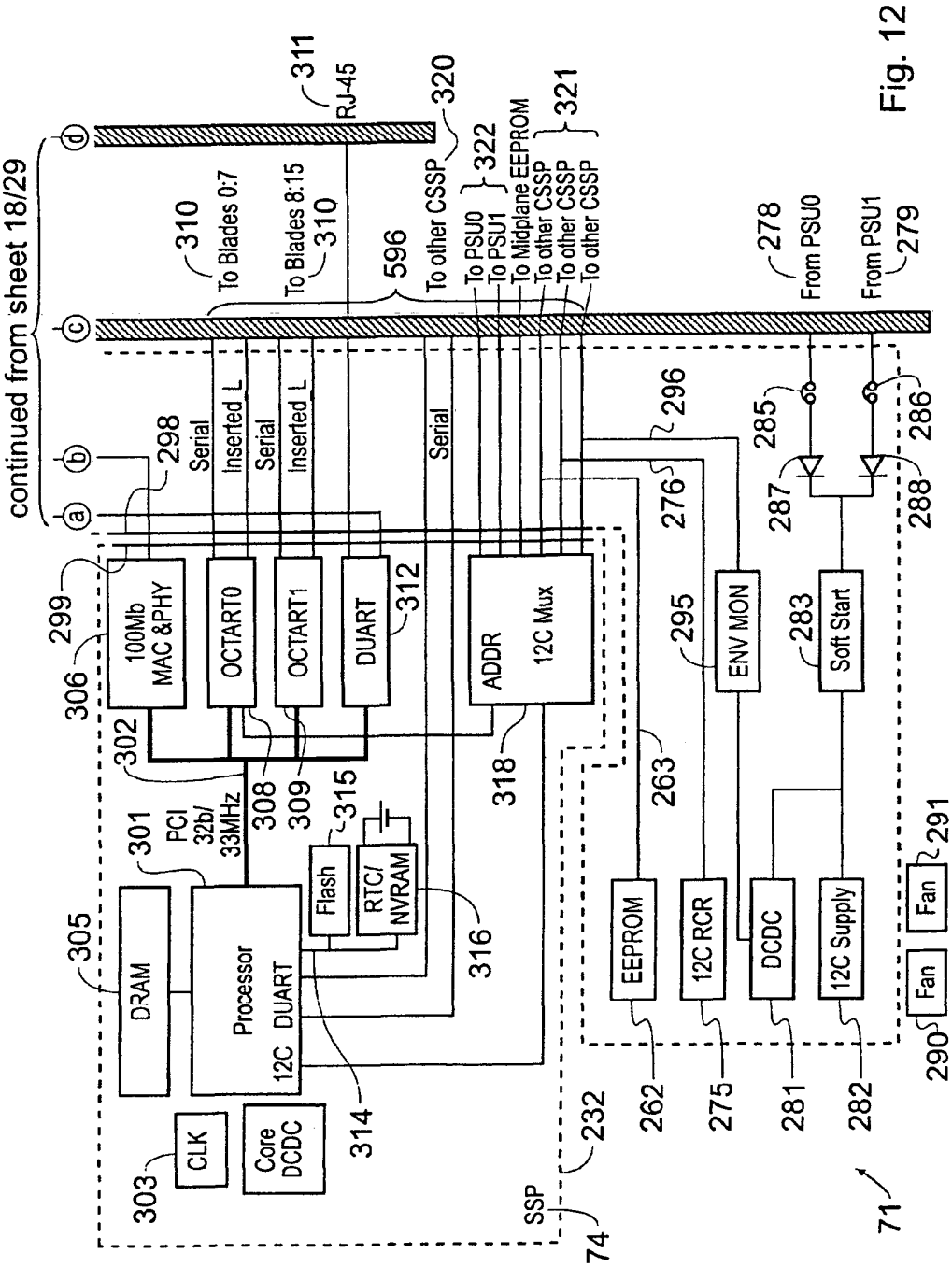

continued from sheet 18/29
RJ-45
311
320
322
321
310
To Blades 0:7
To Blades 8:15
310
596
To other CSSP
To PSU0
To PSU1
To Midplane EEPROM
To other CSSP
To other CSSP
To other CSSP
278
From PSU0
From PSU1
279
298
Serial
Inserted L
Serial
Inserted L
Serial
296
285
286
276
287
288
299
306
100Mb MAC &PHY
OCTART0
OCTART1
DUART
312
ADDR
12C Mux
295
ENV MON
283
Soft Start
302
308
309
315
318
263
301
PCI 32b/ 33MHz
Flash
RTC/ NVRAM
316
305
DRAM
Processor
12C DUART
314
EEPROM
12C RCR
DCDC
12C Supply
291
Fan
Fan
290
CLK
303
Core DCDC
SSP
74
232
262
275
281
282
71

Fig. 12

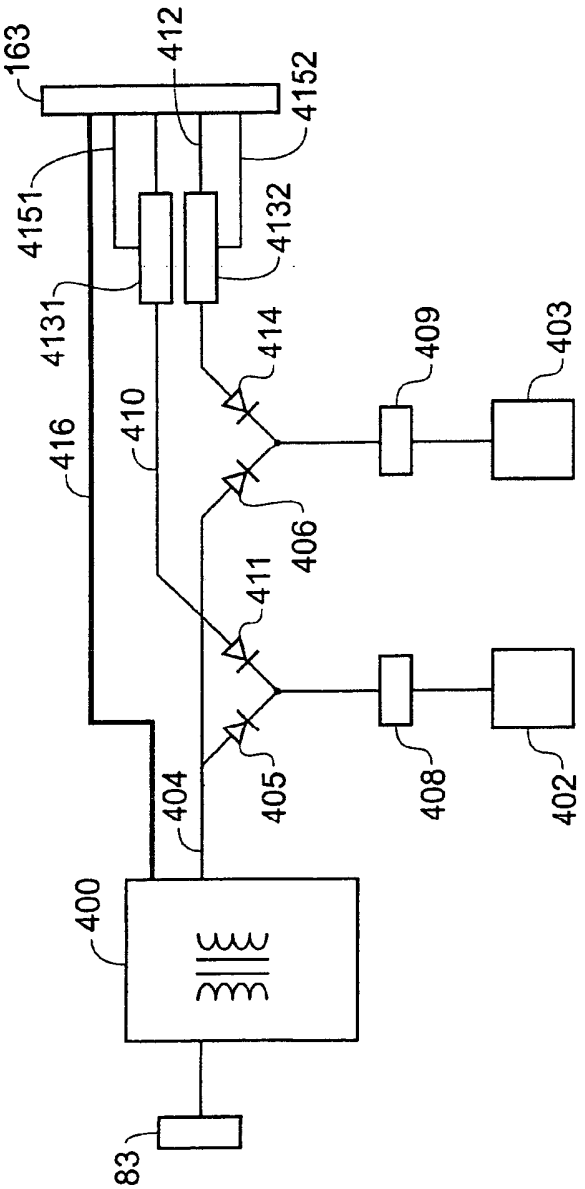

163
412
4152
4151
4132
4131
414
409
403
416
410
406
411
405
408
402
404
400
83

Fig. 13

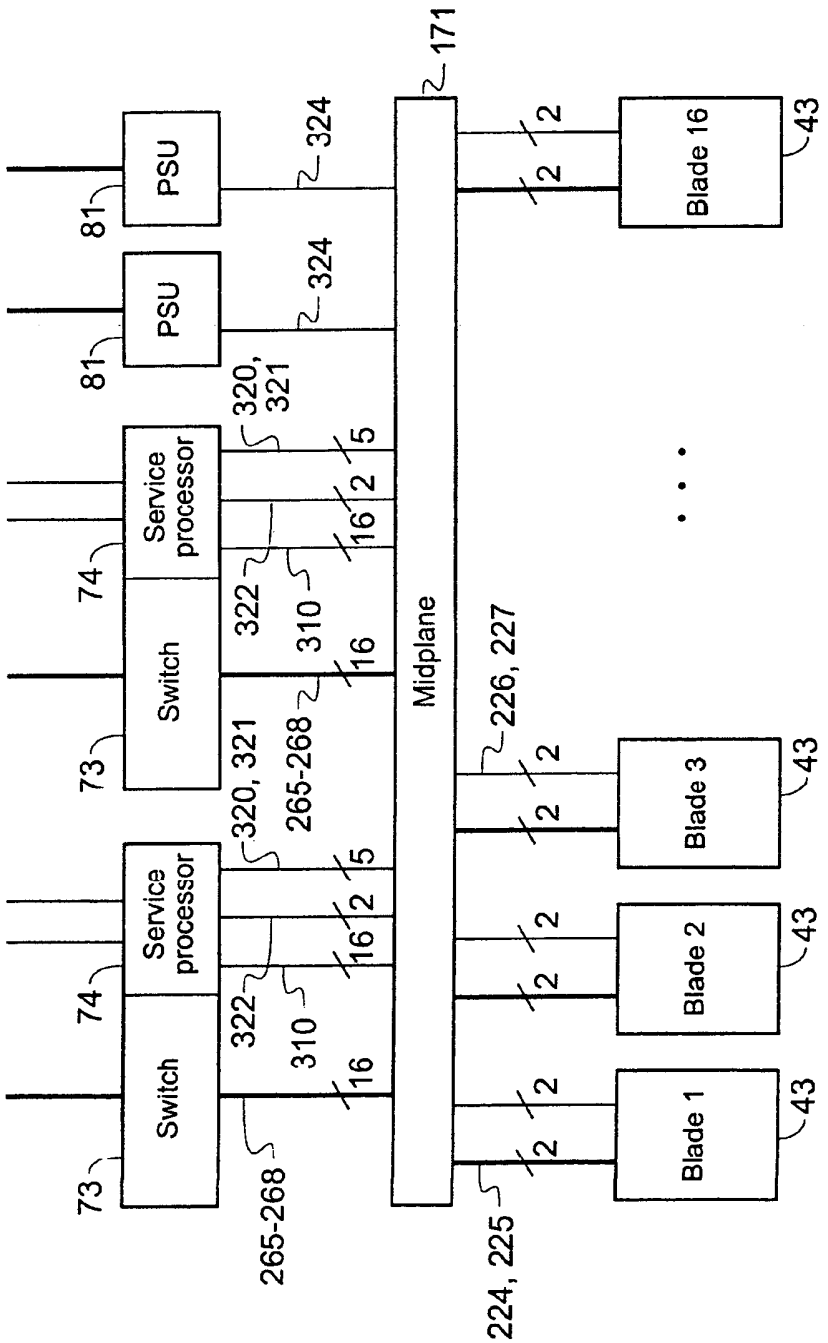

PSU
PSU
81
81
324
324
171
Service processor
Service processor
Switch
Switch
74
74
73
73
320, 321
320, 321
322
322
310
310
265-268
265-268
16
16
2
2
5
5
Midplane
226, 227
224, 225
Blade 16
Blade 3
Blade 2
Blade 1
43
43
43
43

Fig. 14

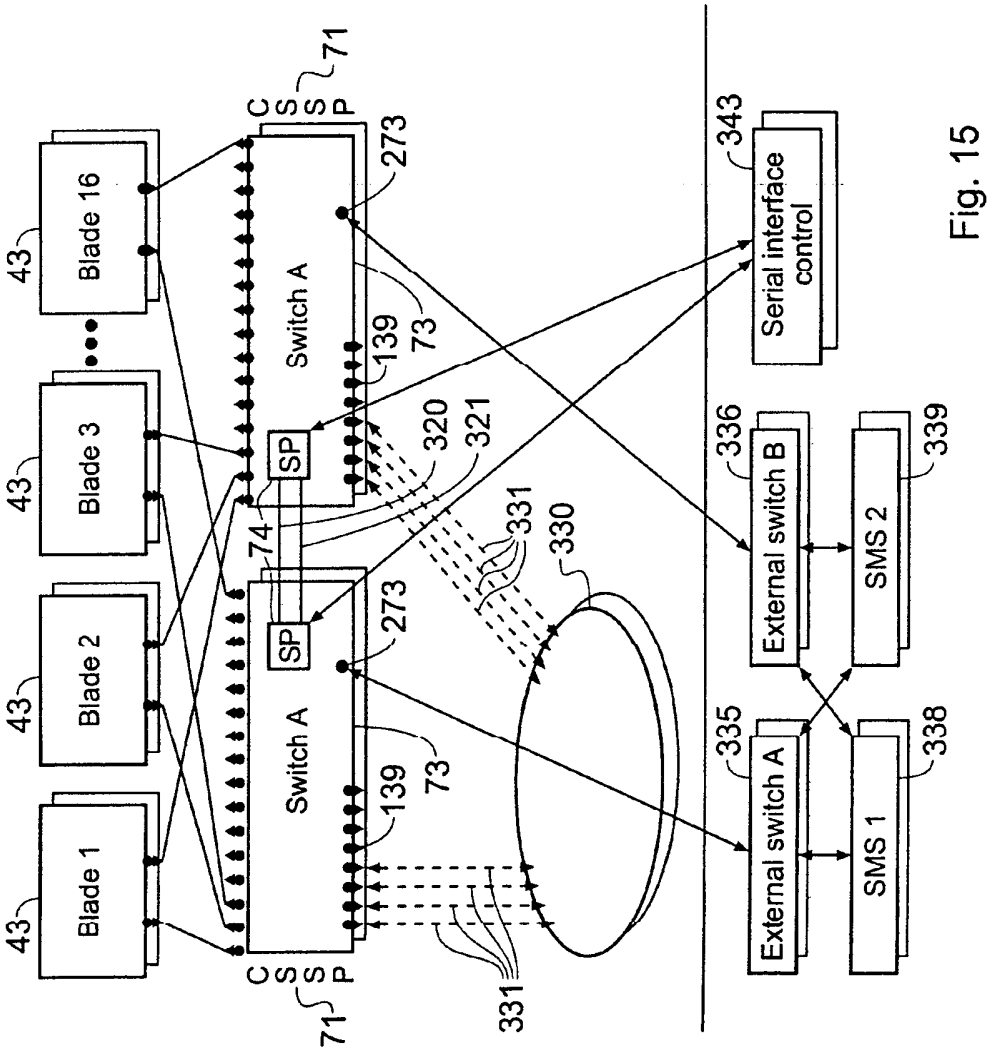

Blade 1
Blade 2
Blade 3
Blade 16
43
Switch A
SP
273
139
73
74
320
321
331
330
71
CSSP
Serial interface control
343
External switch A
External switch B
SMS 1
SMS 2
335
336
338
339

Fig. 15

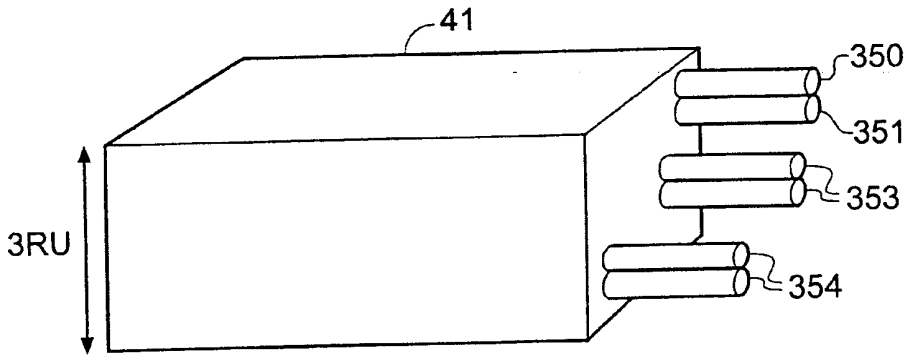


Fig. 16

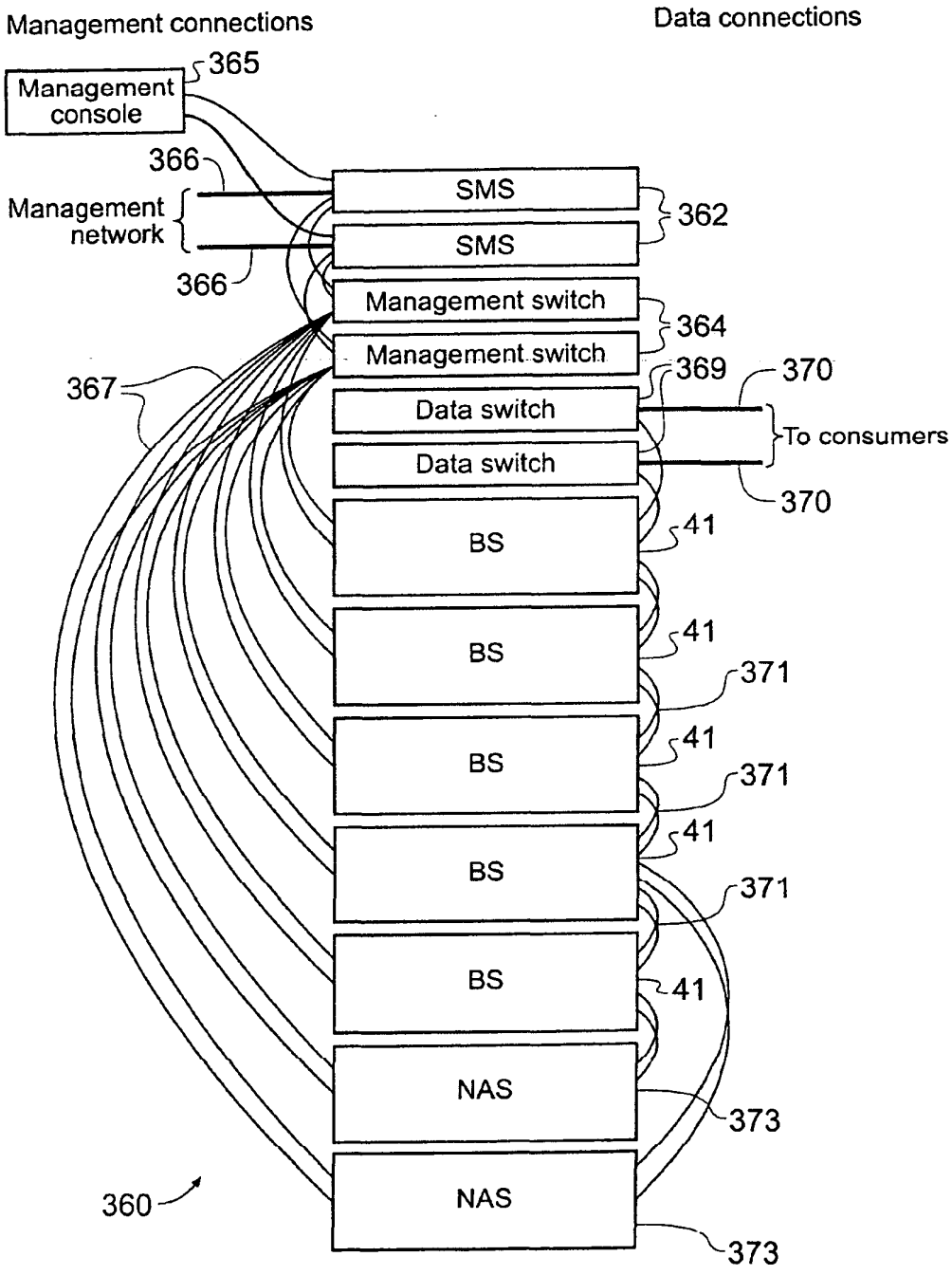

Management connections
Data connections
Management console
365
366
Management network
366
SMS
SMS
362
Management switch
Management switch
364
367
369
370
Data switch
Data switch
To consumers
370
BS
41
BS
41
371
BS
41
371
BS
41
371
BS
41
NAS
373
NAS
373
360

Fig. 17

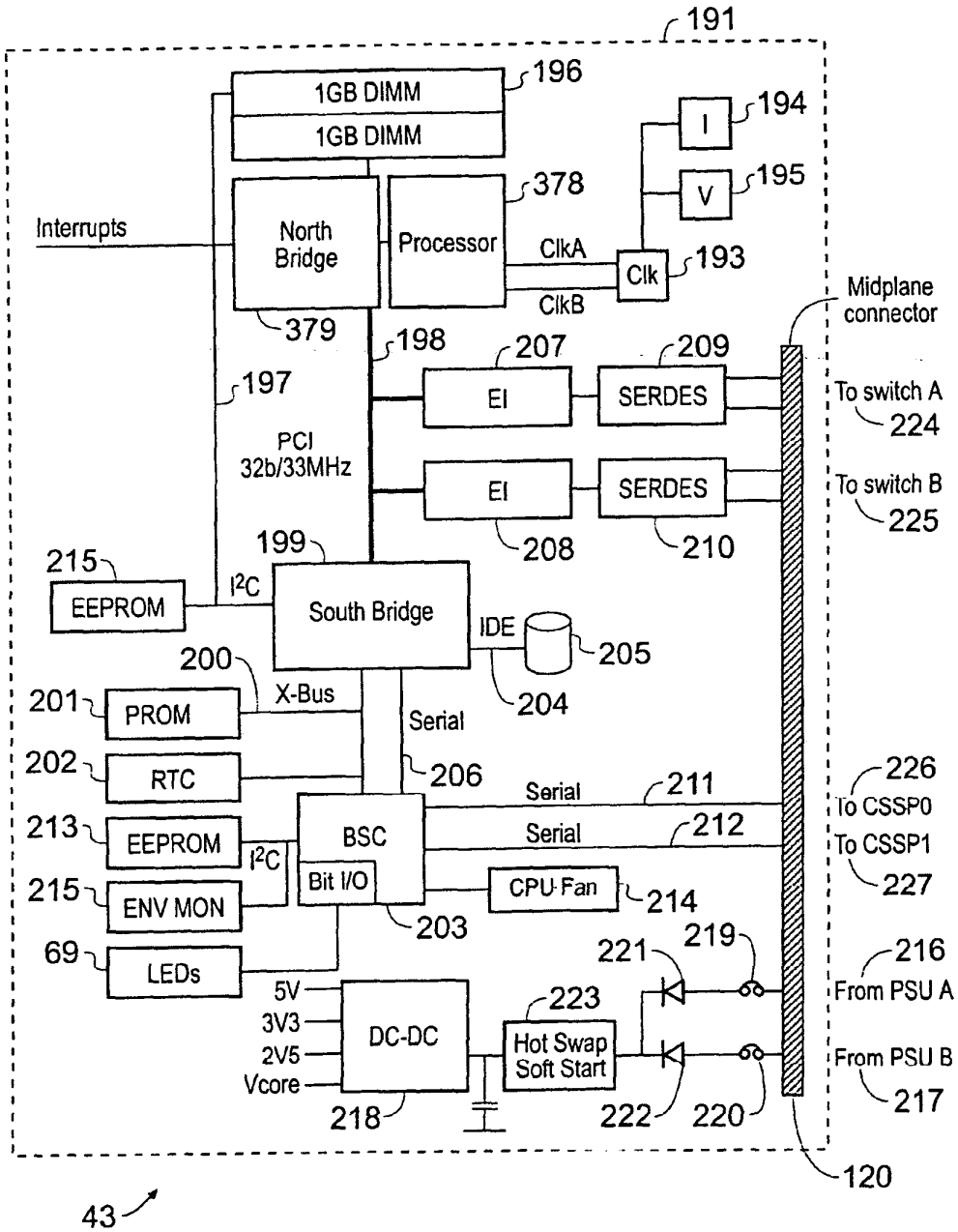

191
1GB DIMM
1GB DIMM
196
I
194
V
195
Interrupts
North Bridge
Processor
378
ClkA
ClkB
Clk
193
379
198
207
209
197
EI
SERDES
Midplane connector
To switch A
224
PCI 32b/33MHz
EI
SERDES
To switch B
225
208
210
199
215
EEPROM
I2C
South Bridge
IDE
205
200
204
201
PROM
X-Bus
Serial
202
RTC
206
Serial
211
226
To CSSP0
213
EEPROM
I2C
BSC
Serial
212
To CSSP1
Bit I/O
227
215
ENV MON
CPU Fan
214
203
221
219
216
69
LEDs
From PSU A
5V
3V3
2V5
Vcore
DC-DC
223
Hot Swap Soft Start
From PSU B
217
218
222
220
120
43

Fig. 18

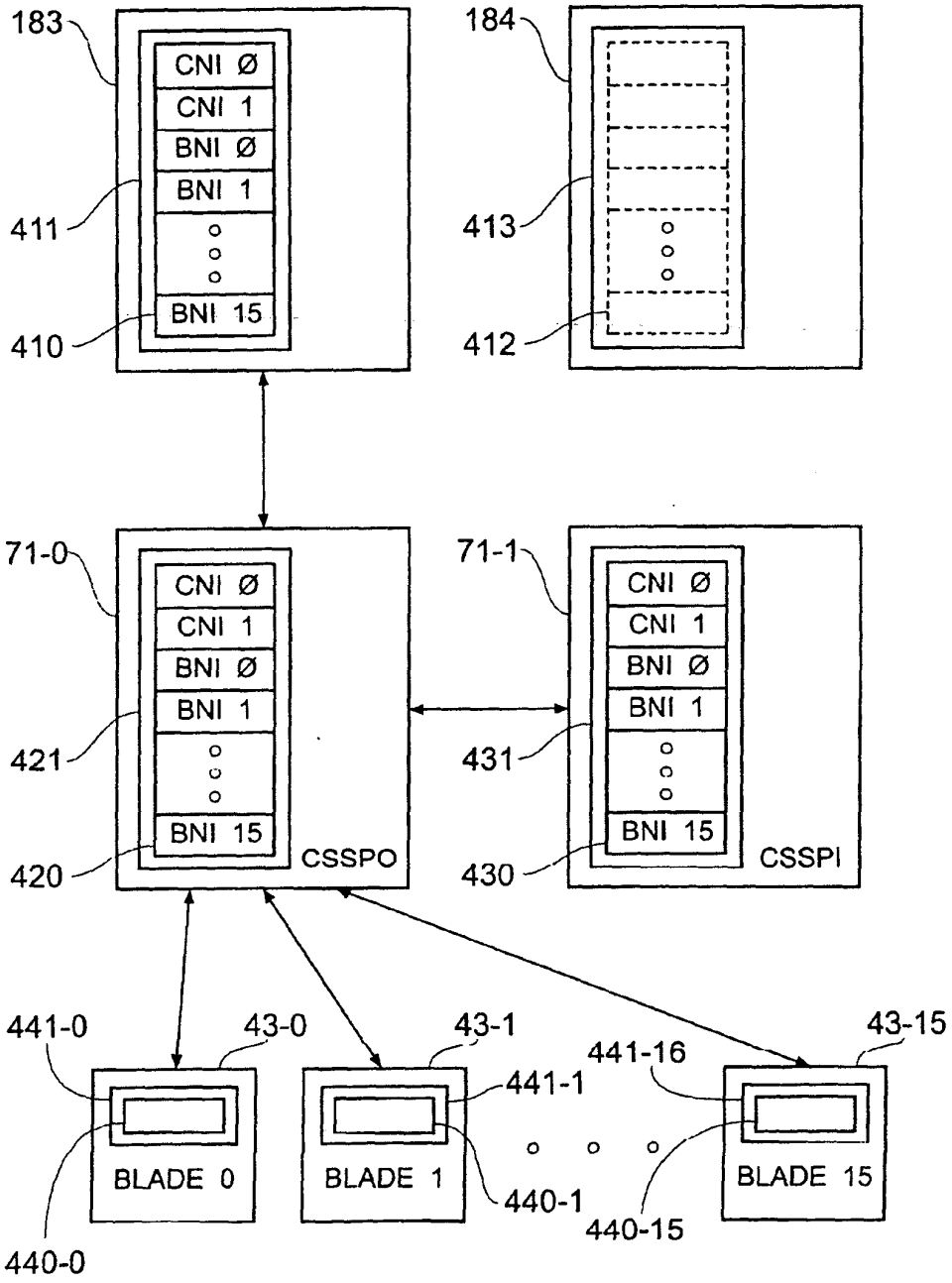

183
CNI Ø
CNI 1
BNI Ø
BNI 1
BNI 15
411
410
184
413
412
71-0
421
420
CSSPO
71-1
431
430
CSSPI
441-0
43-0
43-1
441-16
43-15
441-1
BLADE 0
BLADE 1
BLADE 15
440-1
440-0
440-15

Fig. 19

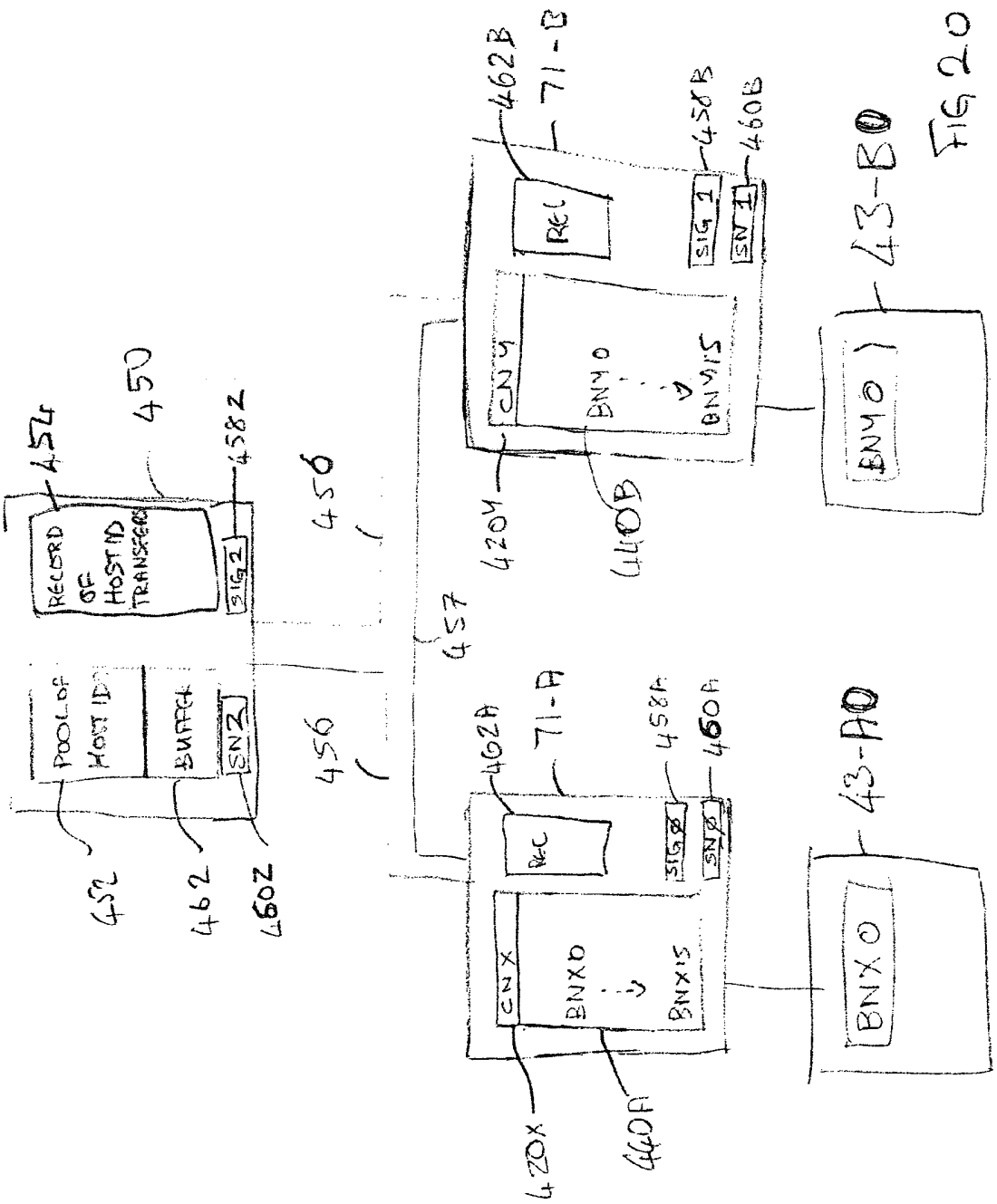

RECORD OF HOST TO TRANSFER
SIG 2
SN 2
POOL OF HOST IDs
BUFFER
452
462
460Z
458Z
454
450
456
457
REC
SIG 1
SN 1
462B
458B
460B
CNY
BNY 0
BNY 15
420Y
440B
71-B
43-B0
BNY 0
REC
SIG 0
SN 0
462A
458A
460A
CNX
BNX 0
BNX 15
420X
440A
71-A
43-A0
BNX 0

FIG 20

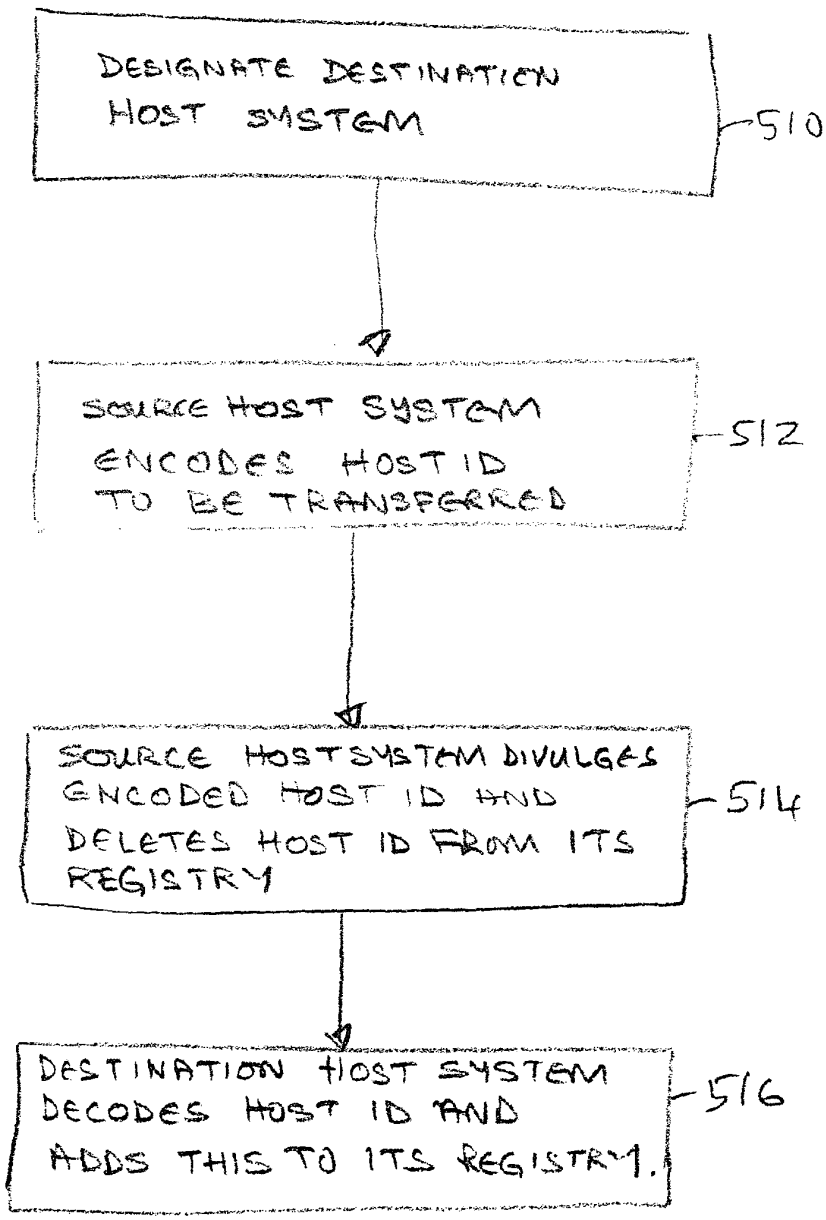

DESIGNATE DESTINATION HOST SYSTEM
510
SOURCE HOST SYSTEM ENCODES HOST ID TO BE TRANSFERRED
512
SOURCE HOST SYSTEM DIVULGES ENCODED HOST ID AND DELETES HOST ID FROM ITS REGISTRY
514
DESTINATION HOST SYSTEM DECODES HOST ID AND ADDS THIS TO ITS REGISTRY.
516

FIG 21

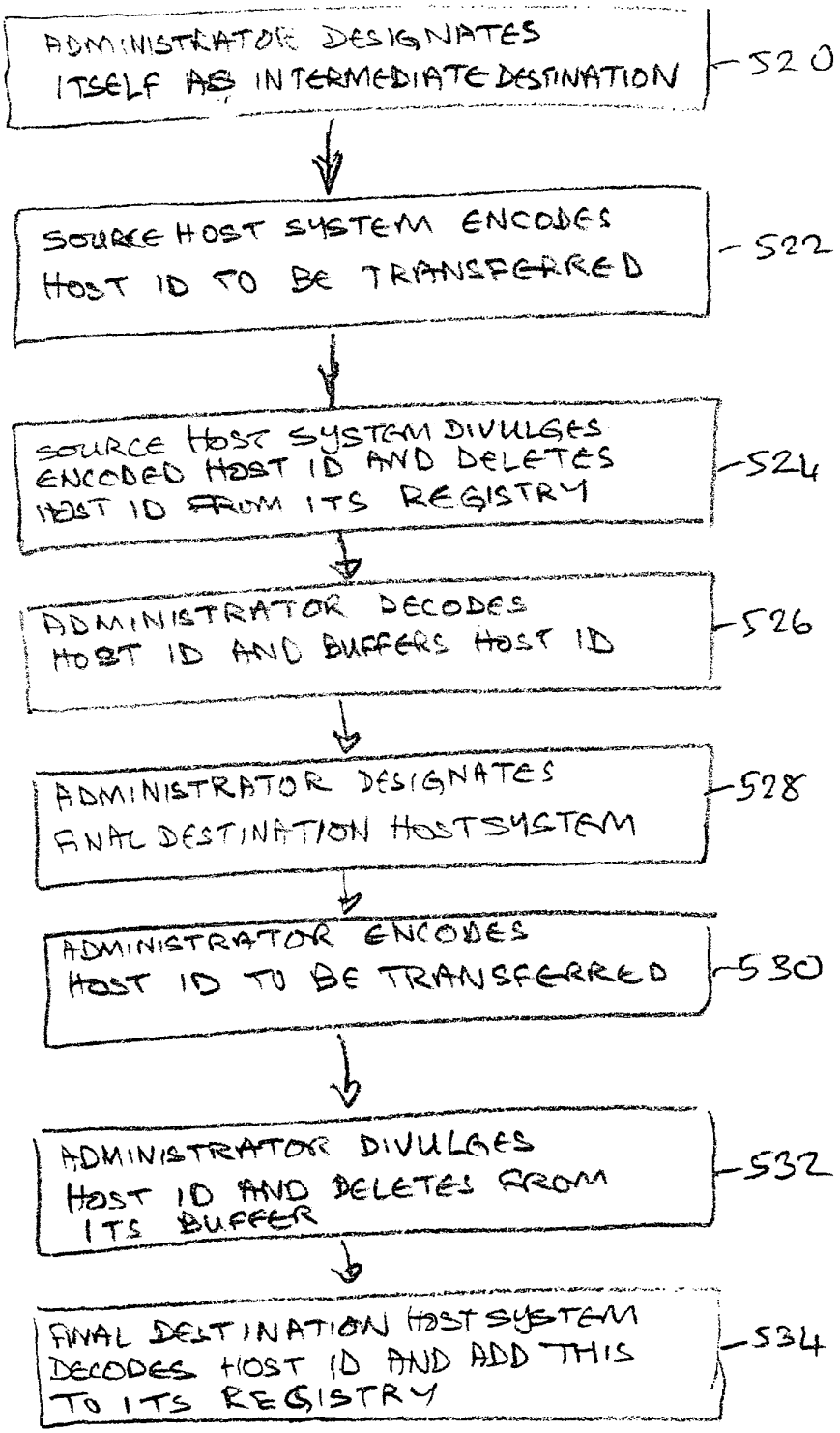

ADMINISTRATOR DESIGNATES ITSELF AS INTERMEDIATE DESTINATION
520
SOURCE HOST SYSTEM ENCODES HOST ID TO BE TRANSFERRED
522
SOURCE HOST SYSTEM DIVULGES ENCODED HOST ID AND DELETES HOST ID FROM ITS REGISTRY
524
ADMINISTRATOR DECODES HOST ID AND BUFFERS HOST ID
526
ADMINISTRATOR DESIGNATES FINAL DESTINATION HOSTSYSTEM
528
ADMINISTRATOR ENCODES HOST ID TO BE TRANSFERRED
530
ADMINISTRATOR DIVULGES HOST ID AND DELETES FROM ITS BUFFER
532
FINAL DESTINATION HOST SYSTEM DECODES HOST ID AND ADD THIS TO ITS REGISTRY
534

FIG 22